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Patent Application

Inventors: Young-Kai Chen et al

Case No.: 28 – 19 – 3 – 3

Serial No.: 10/624,038

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Examiner: Matthew C. Landau

Title: FLAT PROFILE STRUCTURES FOR BIPOLAR TRANSISTORS

Mail Stop: Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REPSONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF UNDER 37 C.F.R. § 41.37

In response to the Notice, Applicants submit replacement sheets for pages 2 – 3 of the Appeal Brief, i.e., sections (i) – (vi) therein. In section (v), the replacement sheet for page 2 identifies the independent claim as claim 8 thereby correcting original page 2.

In the event of a non-payment or an improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 12-2325,** as required to correct the error.

Respectfully,

John McCabe

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Date: Dec. 11, 2007
Alcatel-Lucent
Docket Administrator, Room 2F-192
600-700 Mountain Avenue
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Date of Deposit Dec. 11, 2007

I hereby certify that this correspondence is being deposited with the United States Postal Service First Class Mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated above.

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ITEMS OF APPEAL BRIEF UNDER 37 C.F.R. § 41.37

i) Real party-in-interest

The real party-in-interest is Lucent Technologies Inc., 600-700 Mountain Ave., Murray Hill, NJ 07974-0636. Lucent Technologies Inc. is owner of the entire interest in the application-at-issue by an assignment recorded at Reel/Frame Nos. 014326/0796 on July 21, 2003.

ii) Related appeals and interferences

Appellants do not know of any prior and pending Appeals, Interferences, or Judicial Proceedings related to, directly affecting, directly affected by, or have a bearing on the Board's decision in this Appeal.

iii) Status of claims

Claims 8, 10, 12 – 14, 16 – 19, 22, 25, 29 – 31 are rejected.

Herein, the rejections of all of these claims are appealed.

In the Final Office Action, only pages 2 – 6 state claim rejections. Thus, any earlier claim rejections are either stated on those pages or are assumed waived. See 37 C.F.R. §§ 113(b), 104; M.P.E.P. § 706.07.

iv) Status of amendments

There were no amendments submitted after mailing of the Final Office Action.

v) Summary of claimed subject matter

Independent claim 8 features an integrated circuit (see e.g., Fig. 2 and page 3, lines 24 - 25). The integrated circuit includes a substrate (e.g., substrate 22 in Fig. 2 and at page 3, lines 28 - 31) having a top surface (e.g., surface 23 in Fig. 2 and at page 3, lines 28 - 31) and collector, base, and emitter semiconductor layers (e.g., layers 24, 25, 26 in Fig. 2 and at page 3, lines 28 - 32) of a bipolar transistor (e.g., transistor 20 in Fig. 2 and

at page 3, line 28). The semiconductor layers form a vertical sequence (e.g., sequence 24, 25, 26 in Fig. 2 and at page 3, lines 28 - 32) on the substrate in which intrinsic portions of two of the semiconductor layers (e.g., portion 28 and adjacent part of layer 26 in Fig. 2 and between page 3, line 32, and page 4, line 11) are sandwiched between the top surface of the substrate and a remaining top one of the semiconductor layers (e.g., layer 24 in Fig. 2). The base layer includes an extrinsic portion (e.g., portion 29 in Fig. 2 and between page 3, line 32, and page 4, line 1) that laterally encircles a vertical portion of the top one of the semiconductor layers (e.g., portion 29 and layer 24 in Fig. 2 and page 4, lines 1 - 2). The integrated circuit includes a dielectric sidewall (e.g., spacer 30 in Fig. 2 and at page 4, lines 12 - 13) being interposed between the vertical portion of the top one of the semiconductor layers and the extrinsic portion of the base layer (e.g., layer 24 and portion 29 in Fig. 2 and page 4, lines 12 - 13). The substrate includes a subcollector that forms an electrical contact for the collector layer (layer 27 in Fig. 2 and at page 3, lines 31 – 32, and page 4, lines 2 - 4). The entire subcollector is located outside of the portion of the substrate that is vertically below part of the base layer (see e.g., subcollector layer 27 and right extrinsic portion 29 of base layer 26 in Fig. 2).

vi) Grounds of rejection to be reviewed on appeal

A) Whether claims 8, 10, 12 – 14, 22, and 25 are novel under 35 U.S.C. § 102(b) over U.S. Patent 5,506,427 of Imai et al (Herein, referred to as Imai.).

B) Whether claim 17 is non-obvious under 35 U.S.C. § 103(a) over a combination of Imai as applied to claim 8 and U.S. Patent 5,444,003 of Wang et al (Herein, referred to as Wang.).

C) Whether claims 18 – 19 and 29 – 30 are non-obvious under 35 U.S.C. § 103(a) over a combination of Imai as applied to claim 8 and U.S. Patent 6,541,346 of Malik (Herein, referred to as Malik.).

D) Whether claim 31 is obvious under 35 U.S.C. § 103 over a combination of Imai and Malik as applied to claims 18 – 19 and 29 – 30 and U.S. Patent 5,096,844 of Konig et al (Herein, referred to as Konig.).